IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/630,332	Confirmation No.: 8758
Appellant:	Hyesook Hong	
Filed:	July 30, 2003	
TC/AU:	2812	
Examiner:	Ron Everett Pompey	
Docket:	TI-35165	
Customer No.:	23494	

APPEAL BRIEF

January 26, 2011

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is Appellant's Appeal Brief filed pursuant to the Notice of Appeal dated 10/26/2010 and 37 C.F.R. §41.37.

Real Party in Interest under 37 C.F.R. §41.37(c)(1)(i)

Texas Instruments Incorporated is the real party in interest.

Related Appeals and Interferences under 37 C.F.R. §41.37(c)(1)(ii)

There are no related appeals or interferences known to appellant, the appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

Status of the Claims on Appeal under 37 C.F.R. §41.37(c)(1)(iii)

Claims 9-18, 20, and 21 are pending in this case.

Claims 9-18 and 20-21 stand finally rejected.

Claims 1-8 and 19 are cancelled.

Claims 9-18 and 20-21 are appealed.

Status of Amendments Filed After Final Rejection under 37 C.F.R. §41.37(c)(1)(iv)

No amendments were filed after final rejection.

Summary of Claimed Subject Matter under 37 C.F.R. §41.37(c)(1)(v)

The invention of Claim 9 is a method for monitoring critical dimension (CD) variations of a reticle 100. Referring to FIGURE 1, a reticle layer 110 is provided over a reticle substrate (para. [0018]) and includes each of: a patterned feature area 120a/120b corresponding to a desired circuitry pattern (para. [0021]); and a test pattern area 130a/130b, wherein a portion of the test pattern area is within a step-distance of a portion of the patterned feature area (para. [0024]). Referring to FIGURE 3, a resist material is patterned by stepping the reticle, the patterning including each of the patterned feature area and test pattern area incorporated in the reticle layer (para. [0038]). The resist material is visually inspected for light and dark regions within the test pattern area, where the light and dark regions represent a corresponding variance in the patterned feature area of the resist material (para. [0034] and [0040]). Using the resist material as patterned by the reticle, the feature of a semiconductor device is formed after the visually inspecting step (para. [0042]).

A key to the invention is recognizing that variances in a pattern feature area can be made to appear as light and dark regions in a specially designed test pattern. The light and dark regions of the invention, an example of which is shown in FIG 3, are at a more macro view (viewing multiple step regions) than at a more micro view (individual

elements similar to FIG. 2). A variance is shown in FIG. 3 as one block 320 appearing as a lighter shade of grey (light region) that another block 330 (dark region). Each block corresponds to a step area (para. [0033]-[0034]). The variance in FIG. 3 appears as blocks of various shades of grey (i.e., the light and dark regions) rather than the black and white of a micro view.

The invention of Claim 10 further requires that a first portion 130a of a test pattern area is within a step-distance of a first portion 120a of a patterned feature area and a second portion 130b of a test pattern area is within a step-distance of a second portion 120b of a patterned feature area (FIG 1). A variance between the first and second portions of the test pattern area is indicative of a variance between the first and second portions of the patterned feature area (para [0024]-[0025]).

The invention of Claim 11 further requires that the test pattern area creates a reflective grating in the patterned resist material wherein the reflective grating is configured to provide the light and dark regions if the variance in the patterned feature area exists (para [0029]).

Grounds of Rejection to be Reviewed on Appeal under 37 C.F.R. §41.37(c)(1)(vi)

1. Whether claims 9-18 and 20-21 were properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Kent (US 6,130,016) in view of Krivokapic et al. (US 5,646,870) [hereinafter Krivokapic] and Minobe et al. (US 7,304,791) [hereinafter Minobe].

Arguments under 37 C.F.R. §41.37(c)(1)(vii)

Whether claims 9-18 and 20-21 were properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Kent in view of Krivokapic and Minobe

Appellant respectfully submits that the Examiner improperly rejected claim 9 as unpatentable over Kent in view of Krivokapic and Minobe. In order to form a prima facie case of obviousness, the cited references must teach or suggest all the claim limitations. The combination of Kent, Krivokapic, and Minobe fails to teach or suggest all the claim limitations. Specifically, there is no disclosure or suggestion in the references of visually inspecting resist material for light and dark regions within the test pattern area, the light and dark regions representing a corresponding variance in the patterned feature area of the resist material as required by Claim 9.

Kent teaches using a calibration reticle to optimize the performance characteristics of a stepper (FIG. 4A). The calibration reticle is distinct from the semiconductor structure reticle used to form the semiconductor structure. The test pattern formed using the calibration reticle is inspected by checking the clarity of the pattern and comparing the size and shape of the test pattern to the size and shape of the pattern on the calibration reticle (col. 7 lines 30-35).

Krivokapic teaches an in-scribe area 108 (test pattern) and an in-die area 109 (device pattern) and measuring the critical dimensions of lines in a photoresist layer 118 in an in-scribe area 108 (col. 8 lines, 48-65). Krivokapic further describes the continued process of etching the wafer after the resist pattern is measured.

Minobe teaches an optical microscope and using the optical microscope to view areas on cut samples of a polymer film (col. 16, lines 28-48, col 8, lines 23-36, and FIGs 5-6 for example). Although a test pattern 6 is used for explanation, actual samples

would be observed in practice (Col 17, lines 13-17). Minobe further teaches (Col 8, lines 16-31) that a diffracted light image (dark field) and a direct light image (bright field) can be viewed at the same time to realize relationships between minute defects and large textures.

As noted by the Examiner on page 6, lines 7-11 of the Office Action dated 5/26/2010 and previously argued by the applicant, the combination of Kent and Krivokapic fail to disclose or suggest visually inspecting resist material for light and dark regions within the test pattern area, the light and dark regions representing a corresponding variance in the patterned feature area of the resist material. While Minobe does teach viewing a dark field image and a bright field image simultaneously to observe a relationship between minute defects/foreign matters and large textures, this does not disclose or suggest, in combination with Kent and Krivokapic, visually inspecting a resist material for light and dark regions in a test pattern corresponding to a variance in the patterned feature area. There is nothing in the combined references that suggests light and dark regions in a test pattern of a resist material correspond to a variance in a patterned feature area of a resist material. At most Minobe suggests that you can view the actual defects in an area and the overall texture of that same area at the same time. Only the instant invention provides the recognition that a variance in a pattern feature of a resist material can be observed by inspecting a specially designed test pattern for light and dark regions (i.e., various shades of gray) such as those shown in FIG. 3. Nothing in the combined references suggests this claim feature. Because the combined references fail to teach or suggest each and every element of the claim, the rejection of claim 9 and the claims dependent thereon is improper and should be reversed.

The rejection of Claim 9 is further improper as there is no disclosure or suggestion in the references of providing a reticle layer including each of a patterned feature area corresponding to a desired circuitry pattern and a test pattern area,

wherein a portion of the test pattern area is within a step-distance of a portion of the patterned feature area. Kent teaches using a calibration reticle for the test pattern area and a distinct semiconductor structure reticle for the patterned feature area corresponding to the desired circuitry pattern. Because they are located on separate reticles, they are not part of the same reticle layer and cannot be within a step distance of each other. The Examiner argues (on page 2 of the OA date 5/26/2010) that the lower row of widely spaced patterns 220 of FIG. 3A are the patterned feature area corresponding to the desired circuitry pattern. However, FIG. 3A is a drawing of the calibration reticle only. No portion of the calibration reticle is used to form the desired semiconductor structure. Rather the semiconductor structure reticle is used to form the desired structures in Kent. Krivokapic and Minobe are not applied by the Examiner to teach this feature.

Even if the lower row of patterns 220 on the calibration reticle could somehow be considered a patterned feature area corresponding to the desired circuitry pattern, there is no indication that the upper row of patterns and lower row of patterns are within a step distance. Both FIG. 3A of Kent and FIG 1 of the instant application show a reticle. There is no indication in Kent of what features are located within the same step area/distance.

The rejection of Claims 21 and 18 and the claims dependent thereon is similarly improper and should be reversed.

The rejection of Claim 10 is further improper as the references fail to disclose or suggest a first portion of a test pattern area is within a step-distance of a first portion of a patterned feature area and a second portion of a test pattern area is within a step-distance of a second portion of a patterned feature area, a variance between the first and second portions of the test pattern area being indicative of a variance between the first and second portions of the patterned feature area as required by claim 10. The

Examiner argues (page 3, lines 4-12 of OA dated 5/26/2010) that Kent teaches a first portion of a test pattern area (first row of patterns 220 in FIG 3A) within a step distance of a first portion of a patterned feature area (second row of patterns 220 in FIG. 3A). However, FIG 3A is a drawing of the calibration reticle only (Col. 6 lines 14-26). No patterned feature area is shown in FIG 3A. The patterned feature area is on a separate semiconductor wafer reticle (FIG. 4A and col 6 line 53- col 7 line 9).

Claim 11 is further patentable over the combined references as there is no disclosure or suggestion in the references of the test pattern area creating a reflective grating in the patterned resist material wherein the reflective grating is configured to provide the light and dark regions if the variance in the patterned feature area exists. Kent teaches using spaced lines in a test pattern in the calibration reticle to mimic a pitch value of the semiconductor structure reticle (Co. 6, lines 22-26). There is no suggestion in the references to configure the test pattern to provide light and dark regions if the variance in the patterned feature area exists.

In light of the above, Appellant respectfully requests reversal of the Examiner's rejection of claims 9-18 and 20-21.

Respectfully submitted,

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Claims Appendix under 37 C.F.R. §41.37(c)(1)(viii)

1-8. (Cancelled)

9. (Previously Presented) A method for monitoring critical dimension (CD) variations of a reticle, comprising:

providing a reticle layer over a reticle substrate, said reticle layer including each of:

a patterned feature area corresponding to a desired circuitry pattern; and

a test pattern area, wherein a portion of said test pattern area is within a step-distance of a portion of said patterned feature area;

patterning a resist material by stepping said reticle, the patterning including each of the patterned feature area and test pattern area incorporated in said reticle layer;

visually inspecting said resist material for light and dark regions within said test pattern area, said light and dark regions representing a corresponding variance in said patterned feature area of the resist material,

using said resist material as patterned by said reticle to form the feature of a semiconductor device after said visually inspecting.

10. (Previously Presented) The method as recited in Claim 9 wherein said portion of said test pattern area is a first portion of said test pattern area and said portion of said patterned feature area is a first portion of said patterned area and

wherein said first portion of said test pattern area is within a step-distance of said first portion of said patterned feature area and a second portion of said test pattern area is within a step-distance of a second portion of said patterned feature area, a variance between said first and second portions of said test pattern area being indicative of a variance between said first and second portions of said patterned feature area.

11. (Previously Presented) The method as recited in Claim 9 wherein said test pattern area creates a reflective grating in said patterned resist material, and said reflective grating is configured to provide said light and dark regions if said variance in said patterned feature area exists.

12. (Original) The method as recited in Claim 11 wherein said reflective grating includes a reoccurring line/space structure.

13. (Previously Presented) The method as recited in Claim 12 wherein said reoccurring line/space structure has a pitch of less than about 3/2 a wavelength used in said patterning step.

14. (Previously Presented) The method as recited in Claim 9 wherein said test pattern area is located in a scribe region defined by said patterned feature area.

15. (Previously Presented) The method as recited in Claim 9 wherein said variance is a systematic variance in critical dimension (CD) in said patterned feature area.

16. (Original) The method as recited in Claim 9 wherein visually inspecting said material includes visually inspecting said material using an optical microscope.

17. (Original) The method as recited in Claim 16, further including changing a focus on said optical microscope to cause said light and dark regions to become more or less pronounced.

18. (Previously Presented) A method for making a semiconductor device, comprising:

patterning a resist material by stepping a reticle, wherein said reticle includes each of:

a patterned feature area corresponding to a desired feature of a semiconductor device; and

a test pattern area, wherein a portion of said test pattern area is within a step-distance of a portion of said patterned feature area; and

visually inspecting said patterned resist material for light and dark regions within a corresponding test pattern area, said light and dark regions representing a systematic variance in critical dimension (CD) in said patterned resist material;

using said patterned resist material to form the feature of a semiconductor device after said visually inspecting.

19. (Canceled).

20. (Original) The method as recited in Claim 18 wherein said patterned resist material is used to form multiple features, and wherein said multiple features are electrically contacted to form an operational integrated circuit.

21. (Previously Presented) A method for making a semiconductor device, comprising:

patterning a resist material using a reticle having a plurality of step areas within the reticle, wherein said reticle includes each of:

a patterned feature area corresponding to a desired feature of a semiconductor device; and

a test pattern area, wherein a portion of said test pattern area is within a step-area distance of a portion of said patterned feature area; and

visually inspecting said patterned resist material for light and dark regions, differences in said light and dark regions between said plurality of step areas representing a systematic variance in critical dimension (CD) in said patterned resist material;

using said patterned resist material to form the feature of a semiconductor device after said visually inspecting.

Evidence Appendix under 37 C.F.R. §41.37(c)(1)(ix)

None.

Related Proceedings Appendix under 37 C.F.R. §41.37(c)(1)(x)

None.